

REMARKS:

Claim 1 was presented for examination and was pending in this application. In an Official Action dated June 6, 2004, claim 1 was rejected. Applicants thank Examiner for examination of the claims pending in this application and address Examiner's comments below. Applicants further thank Examiner for acceptance of the Drawings and for consideration of the references cited in the Information Disclosure Statements filed on June 13, 2003, November 18, 2003, and March 26, 2004.

Applicants herein amend claim 1. Claims 2-19 are added. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In amending claim 1, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants have simply corrected typographical mistakes and clarified the claimed invention.

Based on the above Amendment and the following Remarks, Applicants respectfully request that Examiner reconsider the outstanding objections and rejections, and withdraw them.

In the Specification

The Examiner urged Applicants to review the specification for corrections of mistakes of grammatical, clerical, or typographical nature. Applicants herein amend the Specification to provide corrections of this nature. No new matter has been added.

Response to Rejection Under 35 USC 102(e)

In the 3rd paragraph of the Office Action, Examiner has rejected claim 1 under 35 USC § 102(e) as allegedly being anticipated by U.S. Patent No. 6,542,991 to Joy et al. (“Joy”). This rejection is now traversed.

Based on the following Remarks, Applicants respectfully submit that for at least these reasons claim 1 is patentably distinguishable over the cited reference. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

Claim 1 recites a multithreaded computer based system for enabling a command in a first thread to access data in a second thread that comprises, *inter alia*,

- a first set of data storage devices capable of storing a first state of said embedded processor, wherein said first state is the state of the embedded processor during the execution of the first program thread;
- a second set of data storage devices capable of storing a second state of said embedded processor, wherein said second state is the state of the embedded processor during the execution of the second program thread;
- wherein at least said first set of data storage devices includes a control status register for identifying a first target set of data storage devices from which a first source operand of a fetched instruction is to be retrieved and for identifying a second target set of data storage devices to which a first result of an executed instruction is to be stored, wherein at least one of said first or said second target set of data storage devices is included in the second set of data storage devices;

The control status registers in the sets of data storage devices capable of storing the processor state beneficially enable a command to be executed in a current thread associated with a first set of storage devices to access data in another thread that is not being executed and that is associated with the first set of storage devices. Accordingly, the claimed control

status register beneficially allows the currently executing thread to access and store information into the state of a different thread that is not currently being executed.

The Joy reference describes a multiple-thread processor with a single-thread interface that is shared among all the threads. (Joy, Title). The multiple-thread processor described in Joy includes a multi-dimensional register file to increase context-switching performance:

Context-switching performance of the processor 1200 is improved by context-switchable storage structures such as a register file with "windows". The windows support different "contexts" for function calls. In one example, the register file with windows is configured as a multiple-dimensional structure with "planes" for fast context switching.

Joy, col. 30, lines 62-67.

The concept of the multi-dimensional register file 1300 applies to the support of context switching so that the individual planes 1310 represent a separate context. Context switching between microtasks is rapidly accomplished by simply changing the context number, as shown in FIG. 13 as changing the window pointer 1312.

Joy, col. 27, lines 21-26. The multi-dimensional register file of Joy can share registers among adjacent windows:

A calling function has a current calling window 1710 that uses "OUTS" registers 1712 to pass parameters to an adjacent current receiver window 1720 where the registers become "INS" registers 1722 for the receiver. Similarly, on a return from a function call, the receiver can return results through the "INS" registers 1722, which become the "OUTS" registers for the original receiver.

Joy, col. 29, lines 58-64 (emphasis added). That is, the same set of shared physical registers can be addressed with a different window pointer thereby changing their function within the window, from "INS" to "OUTS" and vice versa.

However, Joy does not teach or suggest "a first set of data storage devices" and a second set of data storage devices" capable of storing a first and a second set of states of the

embedded processor, “wherein at least said first set of data storage devices includes a control status register for identifying a first target set of data storage devices from which a first source operand of a fetched instruction is to be retrieved and for identifying a second target set of data storage devices to which a first result of an executed instruction is to be stored, wherein at least one of said first or said second target set of data storage devices is included in the second set of data storage devices.” The window pointers in Joy can only be used to select the current window or context; “an eight-window register file is addressed using three additional lines for specifying a selected one of eight windows.” Joy, col. 28, lines 19-21. Further, Joy specifically describes that data from inactive threads remains frozen when not being executed:

The fast, nanoseconds range context switching is attained by the capability of freezing the pipeline and by passing multiple threads of data through a multiple-threaded structure that stores data for multiple threads concurrently, for example, through usage of multiple-bit flip-flops. Data of an active thread updates the data storage while data in inactive threads remains frozen. Thread switching occurs by switching thread pathways between the updating states and frozen states.

Joy, col. 14, lines 48-56 (emphasis added). This feature of the Joy system is inconsistent with the use of the claimed “control status registers” of Applicants’ invention, which enables “a command in a first thread to access data in a second thread” as recited in claim 1.

In a rejection under 35 U.S.C. §102, each and every claim element must be present in the applied reference. However, Examiner has failed to point out in the cited reference any prior “control status register” as recited in claim 1. Therefore, it is respectfully submitted that the rejection is improper and should be withdrawn.

Conclusion

Applicants have added new claims 2-19 for which Applicants request consideration and examination. Applicants respectfully submit that these are supported by the specification and are commensurate within the scope of protection to which Applicants believe they are entitled.

In sum, Applicants respectfully submit that claims 1 through 19, as presented herein, are patentably distinguishable over the cited references (including references cited, but not applied). Therefore, Applicants request reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
DAVID A. FOTLAND, ET AL.

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By: H. Ribera

Hector J. Ribera, Attorney of Record
Registration No. 54,397
FENWICK & WEST LLP
801 California Street
Mountain View, CA 94041
Phone: (650) 335-7192
Fax: (650) 938-5200
E-Mail: hribera@fenwick.com